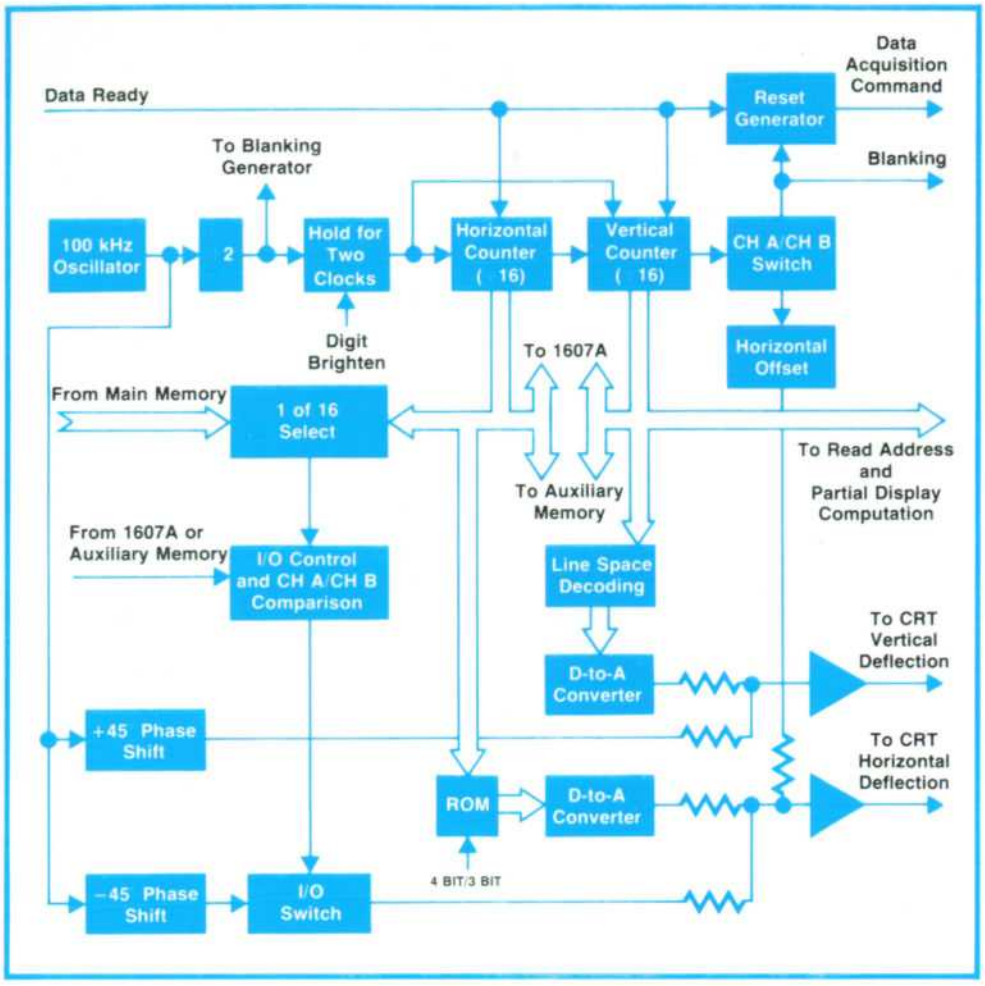

Fig. 7. *Block diagram of the display circuits configured for display of the table of 1's and 0's. When operating in the* REPETITIVE *mode, display cycles repeat until the* DISPLAY TIME *control (not shown) allows the reset generator to issue a data acquisition command. In the* SINGLE *mode, data acquisition is initiated only in response to the front-panel* RESET *button.*

A different method is used for spacing the columns to give the operator a choice of grouping by three's, for octal words, or by four's for hexadecimal words. This is accomplished by using the contents of the horizontal counter to address a ROM, which reads out digital words that generate the appropriate horizontal deflections when applied to the D-to-A converter.

Digits are written on the CRT by adding low-level 100-kHz sine waves to the deflection voltages. The sine waves are shifted 90° with respect to each other so the deflection voltages trace a small ellipse when a "0" is indicated for display. When a "1" is indicated, the sine wave to the horizontal circuits is gated off. Both sine waves are turned off when the instrument displays dots in the MAP mode.

The 100-kHz signal is divided by two to derive the 50-kHz clock for the horizontal counter. It also derives a 50-kHz square wave that blanks the CRT beam for 10 μs while it moves to a new position, and then unblanks it for 10 μs while the digit is written. When a digit is to be brightened for the trigger word or the A & (A $\oplus$ B) mode, the clock input to the counters is interrupted for two clock periods so the digit is written five times before the circuits step to the next digit.

When data from the auxiliary memory is to be displayed, the contents of the vertical and horizontal counters are combined as an eight-bit address for addressing the 256×1-bit RAM. A dc offset voltage is then added to the horizontal deflection to position the auxiliary display to the right of the main display.

Data from a 1607A is displayed on a 1600A by switching the 1600A's horizontal and vertical counters to interrogate the memory in the 1607A. The value of each bit interrogated is returned to the 1600A for display (a multiconductor I/O bus interconnects the two instruments).

Generating the Map Display

When the instrument is operated in the MAP mode, the 16-bit word in memory addressed by the vertical counter is applied directly to the D-to-A converters (Fig. 8). Bits 2 through 7 are applied to the horizontal axis and bits 10 through 15 to the vertical axis. Each word thus appears as a dot at a particular location on the CRT display.

No blanking signals are supplied between dots so the CRT beam traces a line as it moves from dot to dot. To make the lines visible, the display clock rate is slowed to 25 kHz and RC networks are switched into the deflection amplifiers to slow the transient re-